
CS82L41 Schematic and Layout Guidelines

Introduction

This document describes the schematic and layout guidelines for the CS82L41 One-Channel AFE with CMOS Data Output.

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1 General Board Considerations

- Use controlled 50 Ω characteristic impedance for digital signals unless stated otherwise.

2 Layout Guidelines

2.1 Note 1: Device Decoupling

- Place decoupling capacitors close to device on same side of PCB.
- Route VDD_IO decoupling GND to pin 7 (Figure 1).

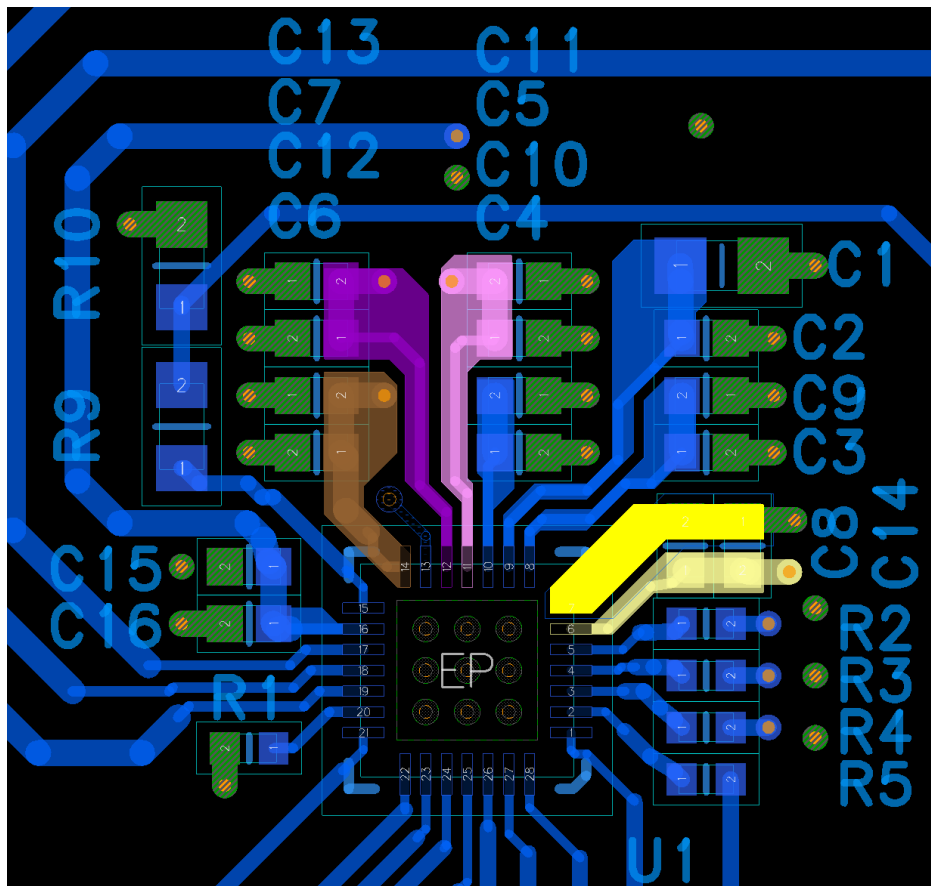


Figure 1 - Device Decoupling with VDD_IO decoupling GND highlighted

2.2 Note 2: Source Termination

- Use termination when system trace lengths justify it.
- Place 33R termination close to device.
- Termination takes second priority to decoupling capacitor placement.

2.3 Note 3: Ground Paddle

- Connect the device's ground paddle to the nearest ground plane with 0.3mm diameter vias on a 3x3, 0.8mm grid.

3 Revision History

Revision History	
Revision	Changes
1.0 APR 2025	Initial version.

Contacting Cirrus Logic Support

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